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1 Register Packing: Exploiting Narrow-Width Operands for Reducing Register File Pressure ■
Oguz Ergin, Deniz Balkan, Kanad Ghose, Dmitry Ponomarev
December 2004 **Proceedings of the 37th annual IEEE/ACM International Symposium on Microarchitecture MICRO 37**
Publisher: IEEE Computer Society
Full text available: pdf(224.06 KB) Additional Information: full citation, abstract

A large percentage of computed results have fewer significant bits compared to the full width of a register. We exploit this fact to pack multiple results into a single physical register to reduce the pressure on the register file in a superscalar processor. Two schemes for dynamically packing multiple "narrow-width" results into partitions within a single register are evaluated. The first scheme is conservative and allocates a full-width register for a computed result. If the computed result tu ...

2 Value-based clock gating and operation packing: dynamic strategies for improving processor power and performance ■
David Brooks, Margaret Martonosi
May 2000 **ACM Transactions on Computer Systems (TOCS)**, Volume 18 Issue 2
Publisher: ACM Press
Full text available: pdf(210.51 KB) Additional Information: full citation, abstract, references, citings, index terms

The large address space needs of many current applications have pushed processor designs toward 64-bit word widths. Although full 64-bit addresses and operations are indeed sometimes needed, arithmetic operations on much smaller quantities are still more common. In fact, another instruction set trend has been the introduction of instructions geared toward subword operations on 16-bit quantities. For examples, most major processors now include instruction set support for multimedia operation ...

3 Real-time shading ■
Marc Olano, Kurt Akeley, John C. Hart, Wolfgang Heidrich, Michael McCool, Jason L. Mitchell, Randi Rost
August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**
Publisher: ACM Press
Full text available: pdf(7.39 MB) Additional Information: full citation, abstract

Real-time procedural shading was once seen as a distant dream. When the first version of this course was offered four years ago, real-time shading was possible, but only with one-of-a-kind hardware or by combining the effects of tens to hundreds of rendering passes. Today, almost every new computer comes with graphics hardware capable of interactively executing shaders of thousands to tens of thousands of instructions. This course has been redesigned to address today's real-time shading capabili ...

4 Proceedings of the SIGNUM conference on the programming environment for development of numerical software
March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1
Publisher: ACM Press
Full text available: pdf(5.02 MB) Additional Information: full citation

5 GPGPU: general purpose computation on graphics hardware
David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn
August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**
Publisher: ACM Press
Full text available: pdf(63.03 MB) Additional Information: full citation, abstract

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

6 The KScalar simulator
J. C. Moure, Dolores I. Rexachs, Emilio Luque
March 2002 **Journal on Educational Resources in Computing (JERIC)**, Volume 2 Issue 1
Publisher: ACM Press
Full text available: pdf(493.35 KB) Additional Information: full citation, abstract, references, index terms

Modern processors increase their performance with complex microarchitectural mechanisms, which makes them more and more difficult to understand and evaluate. KScalar is a graphical simulation tool that facilitates the study of such processors. It allows students to analyze the performance behavior of a wide range of processor microarchitectures: from a very simple in-order, scalar pipeline, to a detailed out-of-order, superscalar pipeline with non-blocking caches, speculative execution, and comp ...

Keywords: Education, pipelined processor simulator

7 Taming the IXP network processor
Lal George, Matthias Blume
May 2003 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation PLDI '03**, Volume 38 Issue 5
Publisher: ACM Press
Full text available: pdf(159.27 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We compile Nova, a new language designed for writing network processing applications, using a back end based on integer-linear programming (ILP) for register allocation, optimal bank assignment, and spills. The compiler's optimizer employs CPS as its intermediate representation; some of the invariants that this IR guarantees are essential for the formulation of a practical ILP model.Appel and George used a similar ILP-based technique for the IA32 to decide which variables reside in registers but ...

Keywords: Intel IXA, bank assignment, code generation, integer linear programming, network processors, programming languages, register allocation

8 Fortran 8X draft
Loren P. Meissner
December 1989 **ACM SIGPLAN Fortran Forum**, Volume 8 Issue 4
Publisher: ACM Press
Full text available: pdf(21.36 MB) Additional Information: full citation, abstract, index terms

Standard Programming Language Fortran. This standard specifies the form and establishes the interpretation of programs expressed in the Fortran language. It consists of the specification of the language Fortran. No subsets are specified in this standard. The previous standard, commonly known as "FORTRAN 77", is entirely contained within this standard, known as "Fortran 8x". Therefore, any standard-conforming FORTRAN 77 program is standard conforming under this standard. New features can b ...

9 VAX floating point: a solid foundation for numerical computation
Mary Payne, Dileep Bhandarkar
June 1980 **ACM SIGARCH Computer Architecture News**, Volume 8 Issue 4
Publisher: ACM Press
Full text available: pdf(979.78 KB) Additional Information: full citation, references

10 A unified vector/scalar floating-point architecture
N. P. Jouppi, J. Bertoni, D. W. Wall
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems ASPLOS-III**, Volume 17 Issue 2
Publisher: ACM Press
Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a unified approach to vector and scalar computation, using a single register file for both scalar operands and vector elements. The goal of this architecture is to yield improved scalar performance while broadening the range of vectorizable applications. For example, reduction operations and recurrences can be expressed in vector form in this architecture. This approach results in greater overall performance for most applications than does the approach of emphasizin ...

11 Avoidance and suppression of compensation code in a trace scheduling compiler
Stefan M. Freudenberger, Thomas R. Gross, P. Geoffrey Lowney
July 1994 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 16 Issue 4
Publisher: ACM Press
Full text available: pdf(3.58 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Trace scheduling is an optimization technique that selects a sequence of basic blocks as a trace and schedules the operations from the trace together. If an operation is moved across basic block boundaries, one or more compensation copies may be required in the off-trace code. This article discusses the generation of compensation code in a trace scheduling compiler and presents techniques for limiting the amount of compensation code: avoidance (restricting code motion so that no compensatio ...

Keywords: SPEC89, instruction-level parallelism, performance evaluation, trace scheduling

12 Pipeline Architecture
C. V. Ramamoorthy, H. F. Li
March 1977 **ACM Computing Surveys (CSUR)**, Volume 9 Issue 1
Publisher: ACM Press
Full text available: pdf(3.53 MB) Additional Information: full citation, references, citings, index terms

13 A Tutorial on Algol 68
Andrew S. Tanenbaum
June 1976 **ACM Computing Surveys (CSUR)**, Volume 8 Issue 2
Publisher: ACM Press
Full text available: pdf(2.92 MB) Additional Information: full citation, references, citings, index terms

14 The horizon supercomputing system: architecture and software
J. T. Kuehn, B. J. Smith
November 1988 **Proceedings of the 1988 ACM/IEEE conference on Supercomputing**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, citings, index terms

Horizon is the name currently being used to refer to a shared-memory Multiple Instruction stream - Multiple Data stream (MIMD) computer architecture under study by independent groups at the Supercomputing Research Center and at Tera Computer Company. Its performance target is a sustained rate of 100 giga (1011) Floating Point Operations Per Second (FLOPS). Horizon achieves this speed with a few hundred identical scalar ...

15 An investigation of static versus dynamic scheduling
Carl E. Love, Harry F. Jordan
May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a
Publisher: ACM Press
Full text available: pdf(1.17 MB) Additional Information: full citation, references, index terms

16 A VLIW architecture for a trace scheduling compiler
Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman
October 1987 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the second international conference on Architectual support for programming languages and operating systems ASPLOS-II**, Volume 15 , 22 , 21 Issue 5 , 10 , 4
Publisher: IEEE Computer Society Press, ACM Press
Full text available: pdf(1.59 MB) Additional Information: full citation, abstract, references, citings, index terms

Very Long Instruction Word (VLIW) architectures were promised to deliver far more than the factor of two or three that current architectures achieve from overlapped execution. Using a new type of compiler which compacts ordinary sequential code into long instruction words, a VLIW machine was expected to provide from ten to thirty times the performance of a more conventional machine built of the same implementation technology.Multiflow Computer, Inc., has now built a VLIW called the TRACE™< ...

17 Improvements to graph coloring register allocation
Preston Briggs, Keith D. Cooper, Linda Torczon
May 1994 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 16 Issue 3
Publisher: ACM Press
Full text available: pdf(2.00 MB) Additional Information: full citation, abstract, references, citings, index terms, review

We describe two improvements to Chaitin-style graph coloring register allocators. The first, optimistic coloring, uses a stronger heuristic to find a k-coloring for the interference graph. The second extends Chaitin's treatment of rematerialization to handle a larger class of values. These techniques are complementary. Optimistic coloring decreases the number of procedures that require spill code and reduces the amount of spill code when sp ...

Keywords: code generation, graph coloring, register allocation

18 A unified decimal floating-point architecture for the support of high-level languages
Frederic N. Ris
September 1977 **ACM SIGPLAN Notices**, Volume 12 Issue 9
Publisher: ACM Press
Full text available: pdf(737.80 KB) Additional Information: full citation, abstract, references

This paper summarizes a proposal for a decimal floating-point arithmetic interface for the support of high-level languages, consisting both of the arithmetic operations observed by application programs and facilities to produce subroutine libraries accessible from these programs. What is not included here are the detailed motivations, examinations of alternatives, and implementation considerations which will appear in the full work.

19 A unified decimal floating-point architecture for the support of high-level languages
Frederic N. Ris
October 1976 **ACM SIGARCH Computer Architecture News**, Volume 5 Issue 4
Publisher: ACM Press
Full text available: pdf(702.74 KB) Additional Information: full citation, abstract, references

This paper summarizes a proposal for a decimal floating-point arithmetic interface for the support of high-level languages, consisting both of the arithmetic operations observed by application programs and facilities to produce subroutine libraries accessible from these programs. What is not included here are the detailed motivations, examinations of alternatives, and implementation considerations which will appear in the full work.

20 An optimizing compiler for lexically scoped LISP
Rodney A. Brooks, Richard P. Gabriel, Guy L. Steele
June 1982 **ACM SIGPLAN Notices , Proceedings of the 1982 SIGPLAN symposium on Compiler construction SIGPLAN '82**, Volume 17 Issue 6
Publisher: ACM Press
Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings, index terms

We are developing an optimizing compiler for a dialect of the LISP language. The current target architecture is the S-I, a multiprocessing supercomputer designed at Lawrence Livermore National Laboratory. While LISP is usually thought of as a language primarily for symbolic processing and list manipulation, this compiler is also intended to compete with the S-1 PASCAL and FORTRAN compilers for quality of compiled numerical code. The S-1 is designed for extremely high-speed signal processing ...

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